CLAIMS

1. A semiconductor device for phase-shifting an input clock using N stages of delay cells each by 1/N clock, selecting a clock which is most synchronized with a reference signal from among clocks outputted from the respective delay cells using a selector, and outputting the selected clock as a sync clock, comprising:

a reference signal phase detection circuit for detecting phase states of a present reference signal and a previous reference signal on the basis of phase differences between the clocks which have been phase-shifted each by 1/N and the present reference signal, and phase differences between the 1/N phase-shifted clocks and the previous reference signal that is one line previous to the present reference signal;

a comparison circuit for comparing the phase states of the present reference signal and the previous reference signal which are detected by the reference signal phase detection circuit;

a phase control circuit for shifting the phase state of the present reference signal to make it coincide with the phase state of the previous reference signal, when the comparison circuit detects that the phase states of the present reference signal and the previous reference signal do not coincide with each other; and

a selector control circuit for controlling the selector on

the basis of the output of the phase control circuit.

2. A semiconductor device as defined in Claim 1 wherein said phase control circuit performs the phase control by counting up the number of clocks stepwisely.

3. A semiconductor device as defined in Claim 1 wherein said phase control circuit performs the phase control by counting down the number of clocks stepwisely.

4. A semiconductor device as defined in Claim 1 wherein said phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1+N)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal.

5. A semiconductor device as defined in Claim 1 wherein said phase control circuit shifts the phase of the clock of the present reference signal at a clock rate interval equivalent to a (1-N)/N clock so as to bring the phase of the present reference signal close to the phase of the previous reference signal.

6. A semiconductor device as defined in Claim 1 wherein said phase control circuit shifts the phase of the clock of the present reference signal so that the clock rate interval becomes

equal to or larger than one clock to bring the phase of the present reference signal close to the phase of the previous reference signal.

7. A semiconductor device as defined in Claim 1 wherein said phase control circuit shifts the phase of the clock of the present reference signal so that the clock rate interval becomes equal to or smaller than one clock to bring the phase of the present reference signal close to the phase of the previous reference signal.

8. A semiconductor device as defined in any of Claims 1 to 7 wherein said phase control circuit counts the number of clocks clock by clock, and performs the phase control on the basis of the count value.

9. A semiconductor device as defined in any of Claims 1 to 7 wherein said phase control circuit counts the number of clocks in units of 1/M-lines (M: integer not less than 2), and performs the phase control on the basis of the count value.

10. A semiconductor device as defined in any of Claims 1 to 7 wherein said phase control circuit counts the number of clocks line by line, and performs the phase control on the basis of the count value.